Claim status:

1. (Previously presented) A phase division multiple access (PDMA) system, the system comprising:

at least one receiver logic combiner, the at least one receiver logic combiner adapted to generate a plurality of relatively prime composite PN codes, wherein each of the plurality of composite PN codes are separated by a predetermined PN phase.

2. (Previously presented) A PDMA system as in claim 1, further comprising at least three first receiver pseudo-noise (PN) component code generators coupled to the at least one receiver logic combiner, wherein each of the at least three first receiver pseudo-noise (PN) component code generators generate relatively prime PN component codes.

3. (Previously presented) A PDMA system as in claim 2 further comprising at least one PN phase delayer coupled to one of the at least three first receiver PN component code generators.

4. (Previously presented) A PDMA system as in claim 2 wherein the at least three first receiver pseudo-noise (PN) component code generators comprise four first receiver PN component code generators.

5. (Previously presented) A PDMA system as in claim 3 wherein the predetermined PN phase substantially equals a phase offset in the relatively prime composite code substantially equal to at least one combination epoch of the relatively prime PN component codes not slipped.

6. (Previously presented) A PDMA system as in claim 1 wherein the receiver logic combiner comprises a MAND logic combiner.

7. (Previously presented) A PDMA system as in claim 1 wherein the receiver logic combiner comprises a MAJ logic combiner.

8. (Previously presented) A PDMA system as in claim 1 wherein the receiver logic combiner comprises a MOD logic combiner.

9. (Cancelled)

10. (Cancelled)

11. (Cancelled)

12. (Cancelled)

13. (Cancelled)

14. (Cancelled)

15. (Cancelled)

16. (Cancelled)

17. (Cancelled)

18. (Cancelled)

19. (Canceled)

20. (Canceled)

21. (Canceled)

22. (Previously presented) A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for generating multi-phase composite pseudo-noise (PN) codes, the method comprising:

generating a first composite PN code, wherein generating the first composite PN code comprises:

generating a plurality of relatively prime PN component codes;

combining the plurality of relatively prime PN component codes;

generating a second composite PN code, wherein the second composite code is PN phase separated from the first composite PN code wherein generating the second composite PN code comprises:

generating the plurality of relatively prime PN component codes;

PN phase delaying one of the plurality of relatively prime PN component codes; and

combining the plurality of relatively prime PN component codes.

23. (Previously presented) A program storage device as in claim 22 wherein the program of instructions comprise at least one Very High Speed Integrated Circuit (VHSIC) Hardware Description (VHDL) Language file.

24. (Previously presented) A phase division multiple access (PDMA) system, the system comprising:

at least one receiver logic combiner, the at least one receiver logic combiner adapted to generate a plurality of relatively prime composite PN codes, wherein each of the plurality of composite PN codes are separated by a predetermined PN phase;

at least three first receiver pseudo-noise (PN) component code generators coupled to the at least one receiver logic combiner, wherein each of the at least three first receiver pseudo-noise (PN) component code generators generate relatively prime PN component codes;

at least one PN phase delayer coupled to one of the at least three first receiver PN component code generators; and

wherein the predetermined PN phase substantially equals a phase offset in the relatively prime composite code substantially equal to at least one combination epoch of the relatively prime PN component codes not slipped.